Novel Three-Level Current-Source PWM Inverter for Photovoltaic Power Conditioner with Grid Connection

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Abstract- This paper presents a new configuration of a three-level current-source PWM inverter (CSI) with a fully common-source topology in terms of all FET switching devices used as a grid connected inverter. Using this common-source CSI, the number of gate drive power supplies can be reduced by using only a single power supply instead of using a conventional bootstrap circuit or isolated power supplies. As a result, it can eliminate expensive transformers and capacitors in the drive circuits of the switching devices. In addition, the circuit can be operated at a higher switching frequency and a higher dv/dt rate because of its common-source topology. The effectiveness of the proposed topology is experimentally verified by using a laboratory prototype set up. Finally, the new inverter circuit is tested for grid connected operation. The experimental results show that the inverter works properly, injecting a sinusoidal current with unity power factor operation.

Keyword: current source inverter, multi-level, power grid

1. INTRODUCTION

Recently, the distributed renewable power generation is becoming more and more popular from the viewpoint of environmental issue and energy conservation. The photovoltaic (PV) solar energy is a very interesting alternative to supplement the generation of electricity among green power sources because it can be utilized either at remote regions as stand alone apparatus or at urban applications with a grid interactive connection [1], [4].

A voltage-source inverter (VSI) such as a three-level neutral-point clamped inverter is conventionally used as a PV power conditioner either for the grid interactive or the standalone operation. This system has limitation when used for a high-voltage and high-switching-frequency application because of a dv/dt problem in the circuit. On the other hand, a current-source inverter (CSI) has some advantages compared with the voltage-source inverter such as no need of an interconnection inductor when used for the grid interactive application, direct controllability of the output current, inherent short-circuit current protection capability and longer lifetime of its reactor if compared with an electrolytic capacitor in the VSI.

Currently, for further practical, reduced dv/dt problem and longer lifetime requirement of the inverter, innovative PV power conditioner circuits should be newly created for the stand alone or the grid interactive operation. General circuit of multilevel CSI has been proposed in [3]. Reference [2] reported the multilevel CSI driven by single gate power supply only at the inverter side. However, the power switches of its chopper still need isolated drive circuits.

In this paper, a new three-level current-source PWM inverter used as a grid connected inverter, which is fully common-source topology at both of the chopper and the inverter circuit is presented. Using this new topology, the number of gate drive power supplies can dramatically be reduced to a single to drive all power switches without isolated power supplies or a conventional bootstrap circuit. In addition, the circuit can overcome the dv/dt problem of the conventional inverters; hence it can be operated at higher voltage and higher switching frequency for better quality of the output current.

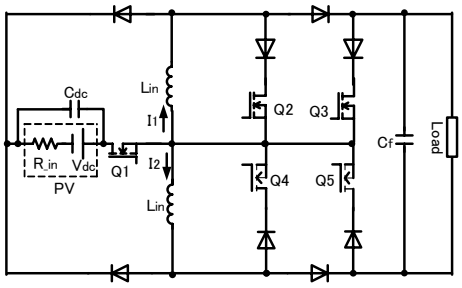


Fig. 1. Proposed common-source three-level CSI circuit.

2. CIRCUIT TOPOLOGY AND OPERATION PRINCIPLE

One of the main goals of the PV power conditioner is to process the PV power into a sinusoidal current to be injected into the utility grid. Such a low distorted current is obtained using proposed three-level current-source inverter as shown in Fig. 1. The current source, at the input of the dc-to-dc converter, is composed by some PV arrays connected to input inductors (L_{in}). As the optimum current of PV is determined by its short-circuit current, photovoltaic is modeled by a simple DC voltage source

(V_{dc}) connected in series with its internal resistance ($R_{\_in}$) [5]. A power decoupling capacitor C_{dc} is connected across the output terminals of the PV arrays to reduce the voltage ripple of the PV arrays. Blocking diodes are placed between the input inductors and the negative terminal of the decoupling capacitor in order to prevent the current from flowing back during positive and negative cycles.

2.1. Chopper Circuit

For an analytical purpose of the buck chopper circuitry, we can consider this circuit comprises two buck choppers with commonly controlled switch (Q1). The chopper behaves as a current source where during positive and negative cycle, a part of the input inductor current (I_{Lin}) will flow back through the blocking diode (I_D) while the switch Q1 is on and the remaining current (I_L) will flow into the inverter during an off-state of the switch Q1.

A current controller is applied to regulate the currents flowing into the input inductors (L_{in}) and amplitude of the output current (I_{pwm}) simultaneously. Making the input inductors current (I_{Lin}) and the output current (I_{pwm}) follow the reference current (I_{ref}) is the objective of this current controller. The switching gate signal of the switch Q1 (dc-to-dc switch) is generated by comparing the error signal of the average value of detected steady state current flowing through both of the input inductors I_1 and I_2, and a triangular carrier wave after passing through a proportional integral (PI) regulator. This signal is used to control the duty cycle of the chopper to obtain balanced input inductor currents I_1 and I_2. In order to avoid uncontrolled state of the output current by modulation signal during the on-state of the switch Q1, the switching time between switch Q1 and the inverter switches must be synchronized as shown in Fig. 2.

When the chopper switch is on for a period of DT, the input inductor is charged by photovoltaic energy to its maximum energy W expressed as

$$W = \frac{1}{2} L_{in} I_{Lin}{}^2. \tag{1}$$

In case of a pure resistive load R_L, the input inductor current I_{Lin} is expressed as

$$I_{Lin} = \frac{V_{pv}}{R_{in}}(1 - e^{-\frac{R_{in} t}{L_{in}}}), \tag{2}$$

where V_{pv} and R_{in} are the terminal output voltage and the internal resistance of photovoltaic system, respectively.

The current increases exponentially to its maximum value, depending on the terminal output voltage of the photovoltaic (V_{pv}) and its internal resistance (R_{in}). This current is the short-circuit current of the photovoltaic. In this calculation, the internal resistance of the input inductor is neglected because its value is much smaller than that of the photovoltaic arrays (R_{in}). The energy is stored in a magnetic field of the input inductor, and when the chopper switch Q1 is off, during (1-DT), the stored energy is discharged to the load via the inverter circuit as a PWM current, where D is the duty cycle of the chopper. The

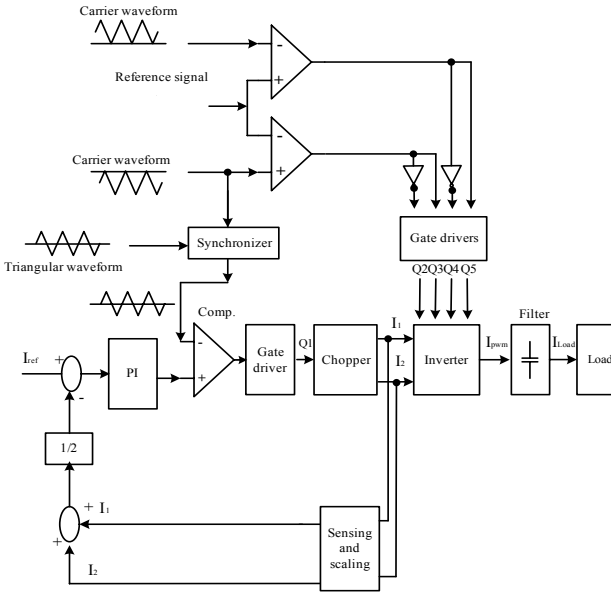


Fig. 2. Block diagram of current controller.

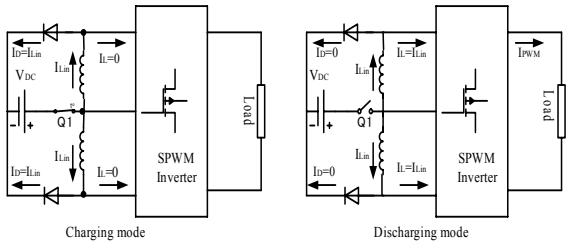


Fig. 3. Operation modes of chopper circuit.

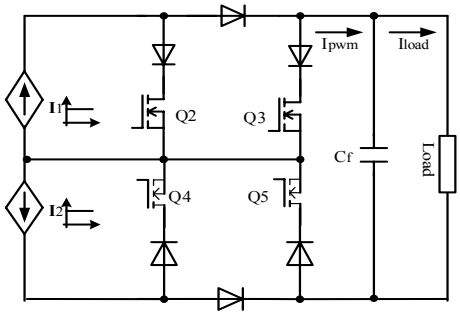


Fig. 4. Equivalent circuit diagram of proposed inverter.

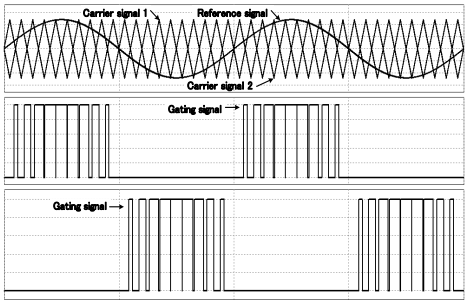


Fig. 5. Sinusoidal PWM for three-level current generation.

on-state circuit or the inductor's energy charging mode and energy discharging mode of the input inductor in this circuit can be represented in Fig. 3. From this figure, the current flowing into the inverter (I_L) can be expressed as

$$I_L = i_{L0} e^{-\frac{R_L}{L_{in}} t}, \quad (3)$$

where i_{Lo} is the initial current flowing through the input inductor. From this equation, it can be found that the current decreases, depending on the time constant of input inductance (L_{in}) and the load resistance (R_L).

2.2. Inverter Circuit and Modulation Strategy

The inverter circuit consists of four controlled switches and six diodes as shown in its equivalent circuit of Fig. 4, where I_1 and I_2 represent the steady state input inductor currents. The diodes connected in series with switching devices are used to protect them from transient voltage due to the load current switching. Sinusoidal pulse width modulation (SPWM) is used to generate the three-level output current pattern with line-frequency (50 or 60 Hz).

The gating signals of the inverter switches are generated by using a sinusoidal reference wave modulated with two triangular carrier waves with the same frequency but with opposite offset values as shown in Fig. 5. This strategy is able to perform the sinusoidal PWM of the inverter. These signal patterns are used to control the inverter switches Q2, Q3, Q4, and Q5. The frequency of the reference signal determines the output current frequency of the inverter and its magnitude can be controlled by the amplitude of the fundamental current component.

The required three-level output current (positive, zero and negative levels) are generated as follows:

1) Positive-level current: Q5 is on, connecting the input inductor current (I_1) to the load. Q4 is on, making the current path for input inductor current (I_2). Q2 and Q3 are off.
2) Zero-level current: Q2 and Q4 are on, making the current path for current I_1 and I_2, respectively. Switches Q3 and Q5 are off.
3) Negative-level current: Q3 is on, connecting the current I_2 to the load. Q2 is on, making the current path for input inductor current (I_1). Q4 and Q5 are off.

The inverter switching frequency is chosen to achieve low noise as well as small harmonic components of the output current and a smaller size of an output current filter by pushing the switching harmonic component to a higher frequency range.

3. EXPERIMENTAL RESULTS

In order to verify and to prove the proposed configuration, a laboratory prototype was set up with 300-V 30-A FK30SM-6 power MOSFETs and 1200-V 16-A HFA16PB120 fast recovery diodes. The experimental circuit specifications are listed in TABLE I. Fig. 6 shows some experimental waveforms, where the three-level output current waveform is indicated in Fig. 6(a). Its FFT analysis result is shown in Fig. 6(b). As can be seen in this result, most of the harmonic amplitudes are less than 3%. The total harmonic distortion of this three-level output current is 5.48%. Fig. 6(c) show the load current after filtering. The current waveform is almost perfect sinusoidal with very small distortion (THD = 0.67%). Fig. 7 shows the current flowing in both the input inductor 1 and the input inductor 2.

TABLE I
CIRCUIT PARAMETERS AND TEST CONDITIONS

Component	Type or value
Input voltage	120 V
PV internal resistance	10 Ω
Input inductor	100 mH
Decoupling capacitor	220 μF
Chopper switching frequency	10 kHz
Inverter switching frequency	30 kHz
Filter capacitor (C_f)	220 μF
Load (R_L,L_L)	R_L = 5.5 Ω, L_L = 3.4 mH
Modulation Index	0.9

TABLE II
GRID CONNECTED TEST CONDITIONS

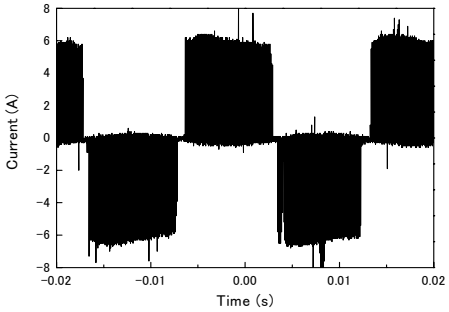
Input voltage	DC 200 V
Input inductor	100 mH
Output filter	C = 2 μF, L = 870 μH, and R = 2 Ω
Power grid	AC 100 V

4. GRID CONNECTED OPERATION TEST

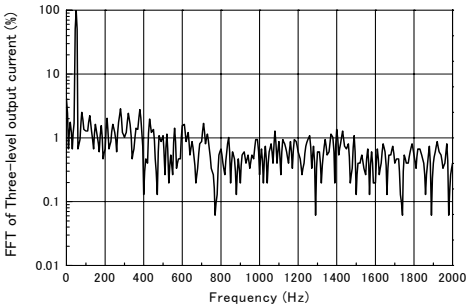
In this section, the experimental results of proposed inverter during grid connected operation are presented. The experimental condition is listed in TABLE II. Fig. 8 shows the inverter output current and the voltage of power grid during experiment. The inverter injects a sinusoidal output current into the power grid with unity power factor operation. Fig. 9. shows the harmonic profile of the injected inverter output current during grid connected operation.

5. CONCLUSION

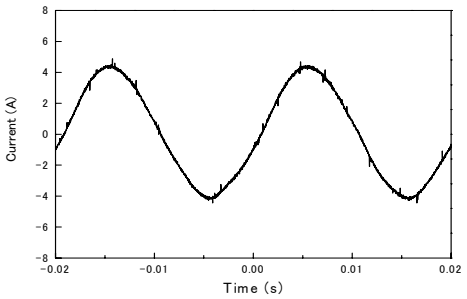
In this paper, a three-level current-source inverter with a fully common-source topology at both of the chopper and inverter sides is experimentally verified. Using this new current source inverter topology, the number of the gate drive power supplies can dramatically be reduced to only a single to drive all power switches. The inverter works well injecting sinusoidal current with unity power factor during grid connected operation.



(a) Three-level output current waveform.



(b) Frequency spectra of three-level output current.



(c) Load current waveform.

Fig. 6. Experimental result of three-level common-source CSI.

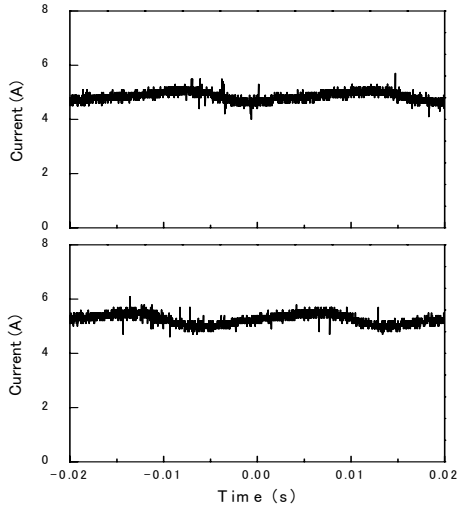


Fig. 7. Input inductor current 1 and 2 of inverter.

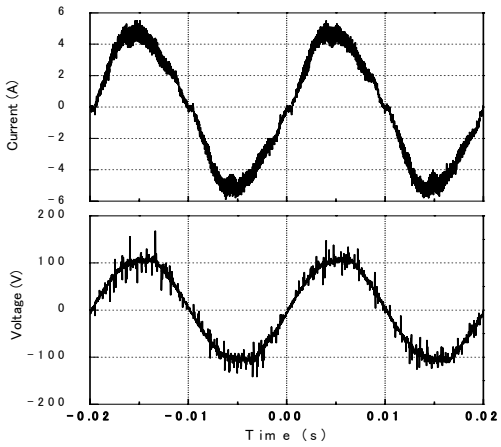


Fig. 8. Inverter output current and grid voltage

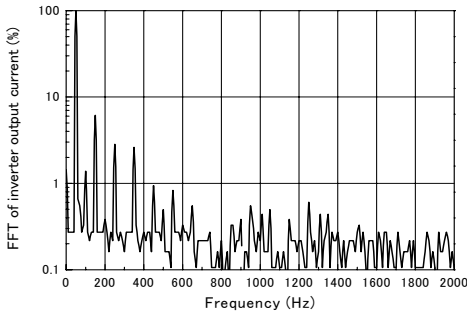


Fig. 9. Harmonic profile of inverter injected current.

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