High-Speed Current Vector Control of PWM Inverter Minimizing Current Error at Every Sampling Point

Toshihiko Noguchi, Hirokazu Kodachi
Nagaoka University of Technology
1603-1 Kamitomioka, Nagaoka,
Niigata 940-2188, JAPAN
tnoguchi@vos.nagaokaut.ac.jp, kodachi@stn.nagaokaut.ac.jp

Isamu Saito
Toshiba Corporation
Information and Industrial Systems & Services Company
1-1-1 Sibaura, Minatoku, Tokyo 105-8001, JAPAN
isamu.saito@toshiba.co.jp

***Abstract* – This paper proposes a novel digital current control technique of a PWM inverter. The key feature of this method is minimization of a current error vector norm at every sampling point with no predetermined current error tolerance, such as a spatial circular area or hysteresis bands. In order to make the current vector trajectory until the next sampling point as close as possible to a predicted current command vector, one of the six non-zero-voltage vectors is appropriately selected in the inverter. A zero-voltage vector is inserted once a sampling period to adjust the current vector velocity and to move the current vector to the closest position to the predicted current command vector. Although manipulating variables in the current loop during the sampling period are limited by the discrete voltage vectors as described above, the proposed method achieves a dead-beat response in a two-dimensional space without the predetermined current error tolerance. Also, on-line identification of a load inductance is introduced to the system to overcome degradation of the response caused by the parameter mismatch. Resultant data obtained from computer simulations and experiments prove feasibility of the proposed technique.**

I. INTRODUCTION

Three-phase current-controlled inverters have extensively been used in many applications such as ac servomotor controllers, switched ac-dc rectifiers, active filters and so forth [1][2]. Basically, these kinds of inverters have current feedback loops to regulate phase currents detected with Hall-effect CTs. The most common and conventional techniques to regulate the currents are a proportional-integral (PI) element based scheme and a hysteresis comparator based scheme. The former has an advantage over the latter in terms of generation of optimum pulsewidth-modulated (PWM) patterns but has drawbacks in a current response and a steady-state error. The latter has both advantages and disadvantages vice versa; hence it is rather difficult for these techniques to satisfy all requirements at the same time without sacrificing any of the performance indexes described above. In order to overcome such dilemma, several proposals have been made on the basis of sophisticated but complicated approaches. One of the approaches is a method using a spatial circular area as a current error tolerance, which can restrict the current error vector within the predetermined circular area [3]. Another is a dead-beat control based algorithm, which achieves an excellent current response with only one sampling time delay [4]. Also, other several papers have reported modified hysteresis comparator based solutions, e.g., an adaptive hysteresis bandwidth approach and an inverter switching sequence optimisation approach [5][6].

This paper proposes a novel digital current vector control technique, which features minimization of a current error vector norm at every sampling point with no predetermined current error tolerance, such as a spatial circular area or hysteresis bands. The proposed method is a kind of dead-beat control. However, the proposed control is achieved in a two-dimensional space, regarding all control variables as instantaneous spatial vector quantities, while the conventional technique was based on the dead-beat control with respect to time. Also, on-line identification of the load parameter is introduced to the controller to solve problems associated with a parameter mismatch. In this paper, a theoretical aspect of the proposed technique is described and several computer simulation and experimental results are presented to show feasibility of the method.

II. PRINCIPLE OF PROPOSED CURRENT VECTOR CONTROL

A. Current-Controlled PWM Inverter

Fig. 1 shows a schematic diagram of the current control system discussed in this paper. It is assumed that a balanced three-phase inductive load with a back electromotive force (e.m.f.) is connected to the inverter and that load resistance is negligibly small. As shown in Fig. 2(a), the inverter can generate six non-zero-voltage vectors $\boldsymbol{v}_1$ - $\boldsymbol{v}_6$ and two zero-voltage vectors $\boldsymbol{v}_0$ and $\boldsymbol{v}_7$, according to its switching state S_u, S_v and S_w. The inverter output voltage vector $\boldsymbol{v}_n$ is mathematically expressed as follows:

$$\begin{aligned}\boldsymbol{v}_n(k) &= v_{n\alpha}(k) + \mathrm{j}v_{n\beta}(k) \\ &= \sqrt{2/3}\,V_{dc}\left[S_u(k) + S_v(k)e^{\mathrm{j}2\pi/3} + S_w(k)e^{\mathrm{j}4\pi/3}\right],\end{aligned} \tag{1}$$

where $n = 0$ - 7 and $S_u, S_v, S_w = 0$ or 1. As can be seen in (1), $\boldsymbol{v}_1$ - $\boldsymbol{v}_6$ have constant magnitude, which is proportional to the dc-bus voltage V_{dc}, and discrete directions as shown in Fig. 2(a), while $\boldsymbol{v}_0$ and $\boldsymbol{v}_7$ have no magnitude.

Since manipulated variables of this current controller are discrete vectors, it is rather difficult to keep the current error vector norm as small as possible during every switching state of the inverter. A continuous time mathematical expression of the system is as follows:

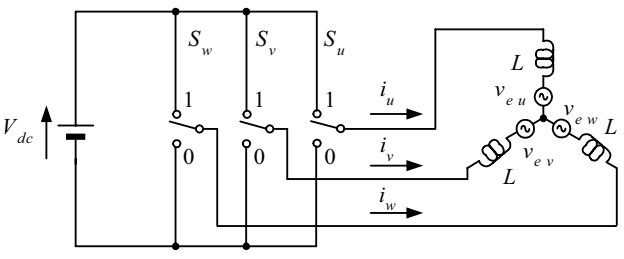

Fig. 1. Current-controlled PWM inverter and load with back e.m.f.

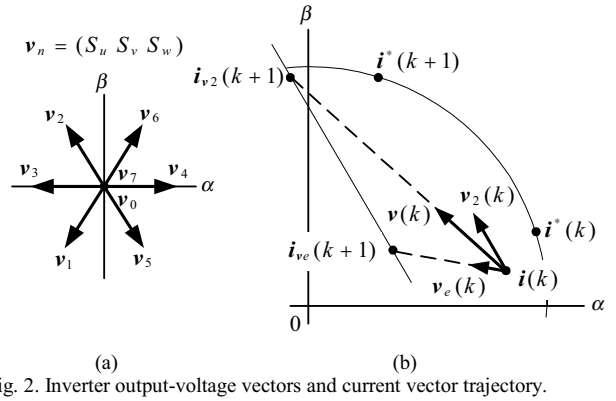

Fig. 2. Inverter output-voltage vectors and current vector trajectory.
(a) Voltage vectors of inverter. (b) Current vector trajectory.

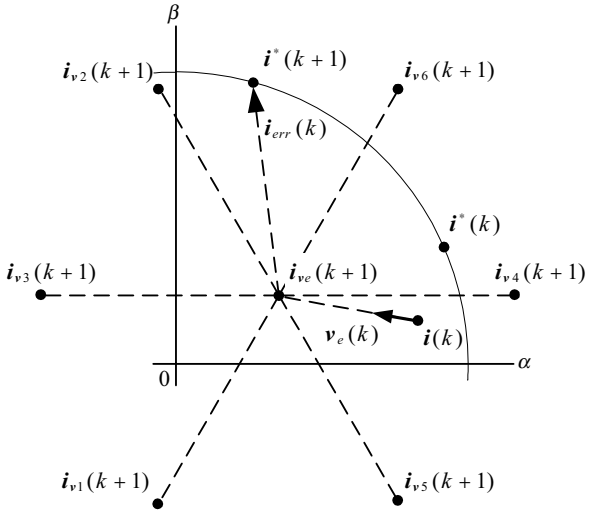

Fig. 3. Possible reachable destinations of current vector.

$$\boldsymbol{v}_n + \boldsymbol{v}_e = L\,\mathrm{d}\boldsymbol{i}/\mathrm{dt}\,. \tag{2}$$

In the above equation, $\boldsymbol{v}_e$ is a back e.m.f. vector of the load. Therefore, the current vector $\boldsymbol{i}$ can be expressed as an integral of sum of $\boldsymbol{v}_n$ and $\boldsymbol{v}_e$. Although $\boldsymbol{v}_e$ is a rotating voltage vector with specific frequency and amplitude, it can be regarded as a constant vector during a sampling period because frequency of $\boldsymbol{v}_e$ is much lower than a sampling rate. Fig. 2(b) shows an example of a current vector trajectory during a sampling period T_s. As can be seen in this figure, if $\boldsymbol{v}_2$ is selected throughout T_s, $\boldsymbol{i}$ proceeds in the direction of $\boldsymbol{v} = \boldsymbol{v}_2 + \boldsymbol{v}_e$ at a constant velocity, which is determined by the switching state, the dc-bus voltage, and the amplitude and the phase of the back e.m.f.

B. Proposed Current Control Algorithm

In many applications of three-phase systems, sinusoidal current waveforms are generally required; thus the inverter discussed in this paper is operated with three-phase sinusoidal current commands given. On this assumption, the proposed current control is executed according to the procedure described below.

1) Acquisition of current command and feedback vectors

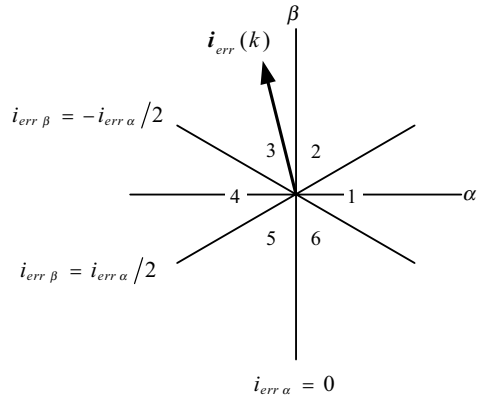

Fig. 4. Spatial sectors to determine current error vector direction.

TABLE I SELECTION OF NON-ZERO-VOLTAGE VECTOR

Sector	Conditions		Vector to select
1	$i_{err\,\alpha} \ge 0$	$-i_{err\,\alpha}/2 < i_{err\,\beta} \le i_{err\,\alpha}/2$	$\boldsymbol{v}_4$
2	$i_{err\,\alpha} \ge 0$	$i_{err\,\beta} > i_{err\,\alpha}/2$	$\boldsymbol{v}_6$
3	$i_{err\,\alpha} < 0$	$i_{err\,\beta} \ge -i_{err\,\alpha}/2$	$\boldsymbol{v}_2$
4	$i_{err\,\alpha} < 0$	$i_{err\,\alpha}/2 \le i_{err\,\beta} < -i_{err\,\alpha}/2$	$\boldsymbol{v}_3$
5	$i_{err\,\alpha} < 0$	$i_{err\,\beta} < i_{err\,\alpha}/2$	$\boldsymbol{v}_1$
6	$i_{err\,\alpha} \ge 0$	$i_{err\,\beta} \le -i_{err\,\alpha}/2$	$\boldsymbol{v}_5$

It is assumed that the following current vector is sampled at a sampling point k:

$$\begin{aligned}\boldsymbol{i}(k) &= i_\alpha(k) + \mathrm{j}i_\beta(k) \\ &= \sqrt{2/3}\left[i_u(k) + i_v(k)e^{\mathrm{j}2\pi/3} + i_w(k)e^{\mathrm{j}4\pi/3}\right].\end{aligned} \tag{3}$$

On the other hand, the current command vector at the next sampling point can be predicted as follows:

$$\begin{aligned}\boldsymbol{i}^*(k+1) &= i_\alpha^*(k+1) + \mathrm{j}i_\beta^*(k+1) \\ &= \sqrt{2/3}\left[i_u^*(k+1) + i_v^*(k+1)e^{\mathrm{j}2\pi/3} + i_w^*(k+1)e^{\mathrm{j}4\pi/3}\right],\end{aligned} \tag{4}$$

where the three-phase current commands are calculated on the assumption that they are sinusoidal, e.g.,

$$\begin{cases} i_u^*(k+1) = I^*\cos\omega^*\left(t+T_S\right) \\ i_v^*(k+1) = I^*\cos\left[\omega^*\left(t+T_S\right) - 2\pi/3\right] \\ i_w^*(k+1) = I^*\cos\left[\omega^*\left(t+T_S\right) - 4\pi/3\right] \end{cases}.$$

2) Detection of load back e.m.f. vector

It is necessary to select an optimum non-zero-voltage vector that allows the current vector $\boldsymbol{i}(k)$ to approach the predicted current command vector $\boldsymbol{i}^*(k+1)$ the most closely. However, the back e.m.f. vector of the load given by (5) prevents $\boldsymbol{i}(k)$ from proceeding in the direction of the selected $\boldsymbol{v}_n(k)$.

$$\begin{aligned}\boldsymbol{v}_e(k) &= v_{e\alpha}(k) + \mathrm{j}v_{e\beta}(k) \\ &= \sqrt{2/3}\left[v_{eu}(k) + v_{ev}(k)e^{\mathrm{j}2\pi/3} + v_{ew}(k)e^{\mathrm{j}4\pi/3}\right]\end{aligned} \tag{5}$$

This back e.m.f. information is usually obtained from sensors, e.g., a rotor position sensor of an ac servomotor and power-source voltage sensors of a switched ac-dc rectifier. As described previously, movement of $\boldsymbol{i}(k)$ is determined by

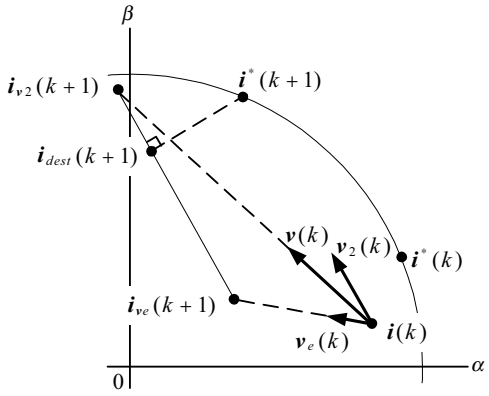

Fig. 5. Optimum destination of current vector.

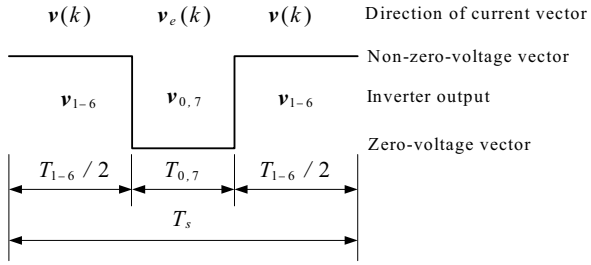

Fig. 6. Switching sequence in one sampling period.

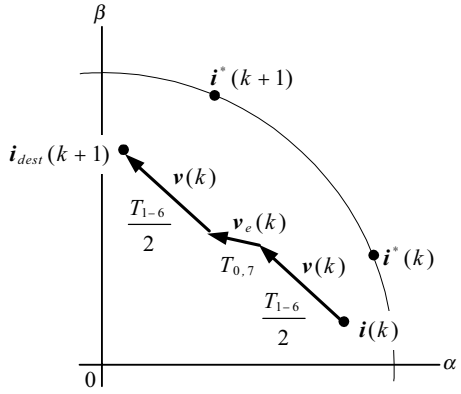

Fig. 7. Scheduled trajectory of current vector.

the sum of $\boldsymbol{v}_n(k)$ and $\boldsymbol{v}_e(k)$ shown by (6). If the inverter output is one of $\boldsymbol{v}_0$ and $\boldsymbol{v}_7$, the direction and the velocity of $\boldsymbol{i}(k)$ are uncontrollable because $\boldsymbol{v}_e(k)$ solely governs movement of $\boldsymbol{i}(k)$. This situation is inherently unavoidable because applying either $\boldsymbol{v}_0$ or $\boldsymbol{v}_7$ is indispensable to control the velocity of $\boldsymbol{i}(k)$.

$$\begin{aligned}\boldsymbol{v}(k) &= \boldsymbol{v}_n(k) + \boldsymbol{v}_e(k) = v_\alpha(k) + \mathrm{j}v_\beta(k) \\ &= v_{n\alpha}(k) + v_{e\alpha}(k) + \mathrm{j}\left[v_{n\beta}(k) + v_{e\beta}(k)\right]\end{aligned} \tag{6}$$

3) Selection of optimum non-zero-voltage vector

Every sampling period T_s is divided into two durations, i.e., duration T_{1-6} of a non-zero-voltage vector and duration $T_{0,7}$ of a zero-voltage vector; hence T_s can be expressed as

$$T_s = T_{1-6} + T_{0,7}. \tag{7}$$

As illustrated in Fig. 2(b), if the non-zero-voltage vector $\boldsymbol{v}_2(k)$ is applied to the load throughout a sampling period, i.e., $T_{0,7} = 0$ and $T_{1-6} = T_s$, $\boldsymbol{v}_2(k)$ allows $\boldsymbol{i}(k)$ to reach the destination of $\boldsymbol{i}_{v2}(k+1)$. On the other hand, if the sampling period is occupied by $T_{0,7}$, i.e. $T_{1-6} = 0$ and $T_{0,7} = T_s$, the destination is $\boldsymbol{i}_{ve}(k+1)$, which is determined by $\boldsymbol{v}_e(k)$. Therefore, a combination of $\boldsymbol{v}_2(k)$ and $\boldsymbol{v}_0(k)$ that satisfies (7) allows the destination of the current vector after T_s to be on a straight line between $\boldsymbol{i}_{v2}(k+1)$ and $\boldsymbol{i}_{ve}(k+1)$.

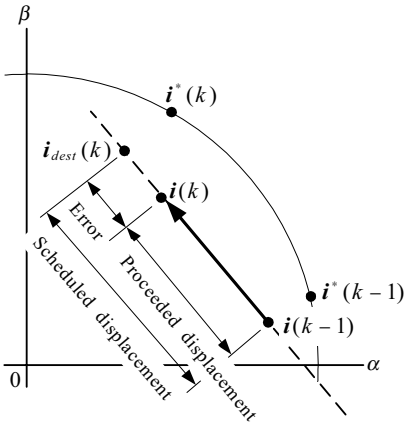

Fig. 8. Principle of inductance identification.

Equation (2) can easily be transformed to a discrete-time expression as follows:

$$\begin{aligned}\boldsymbol{i}_{dest}(k+1) &= \boldsymbol{i}(k) + \left[\boldsymbol{v}_n(k) + \boldsymbol{v}_e(k)\right]T_s / \hat{L} \\ &= \boldsymbol{i}(k) + \boldsymbol{v}_e(k)T_s / \hat{L} + \boldsymbol{v}_{1-6}(k)T_{1-6} / \hat{L}. \\ &= \boldsymbol{i}_{ve}(k+1) + \boldsymbol{v}_{1-6}(k)T_{1-6} / \hat{L}\end{aligned} \tag{8}$$

The above equation represents that the destination of the current vector $\boldsymbol{i}_{dest}(k+1)$ is determined only by $\boldsymbol{v}_{1-6}(k)$ because $\boldsymbol{i}_{ve}(k+1)$ is regarded as a constant vector during the sampling period. Therefore, possible reachable destinations of the current vector can be plotted as shown in Fig. 3, depending on selection of the non-zero-voltage vectors. From the coordinates of $\boldsymbol{i}_{ve}(k+1)$, an optimum non-zero-voltage vector should uniquely be selected, which produces a current vector trajectory closest to the current command vector. For example, if the current error vector $\boldsymbol{i}_{err}(k) = \boldsymbol{i}^*(k+1) - \boldsymbol{i}_{ve}(k+1)$ is closer to $\boldsymbol{i}_{v2}(k+1)$ than $\boldsymbol{i}_{v6}(k+1)$ as illustrated in Fig. 3, $\boldsymbol{v}_2(k)$ is the most appropriate non-zero-voltage vector that makes the current vector trajectory the closest to $\boldsymbol{i}^*(k+1)$. Fig. 4 and TABLE I indicates selection manner of the optimum non-zero-voltage vectors. As shown in Fig. 4, a two-dimensional reference frame of which origin is placed at $\boldsymbol{i}_{ve}(k+1)$ is divided into six sectors to detect the direction of $\boldsymbol{i}_{err}(k)$. The sector where $\boldsymbol{i}_{err}(k)$ belongs can easily be detected by evaluating $i_{err\,\alpha}(k)$ and $i_{err\,\beta}(k)$, and the only one appropriate non-zero-voltage vector is selected according to the sector where $\boldsymbol{i}_{err}(k)$ belongs as described in TABLE I.

4) Calculation of optimum destination of current vector

After selecting a non-zero-voltage vector, e.g., $\boldsymbol{v}_2(k)$, on the basis of Fig. 4 and TABLE I, an optimum destination of the current vector, which is the closest to the predicted current command vector $\boldsymbol{i}^*(k+1)$, is calculated. The destination

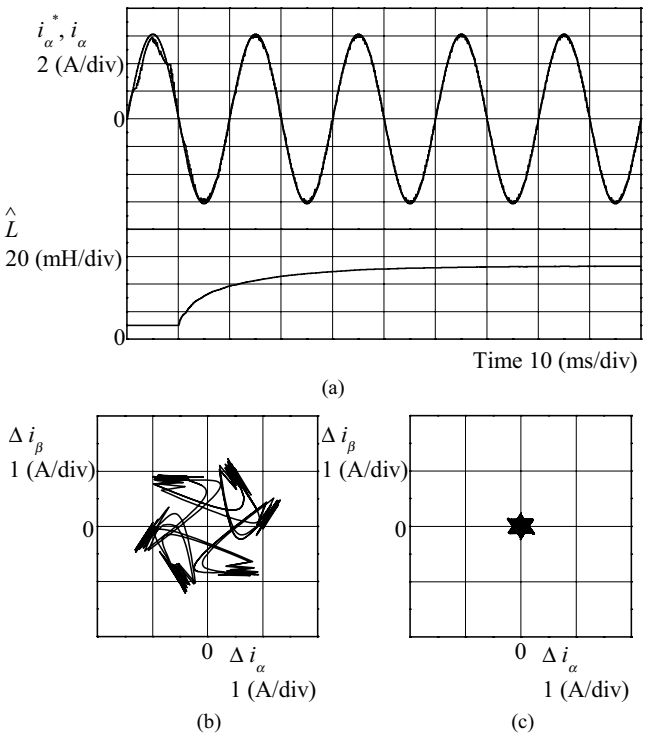

Fig. 9. Simulation result of inductance identification and current error vector loci.
(a) Waveforms of currents and estimated inductance. (b) Current-error vector locus at initial condition. (c) Current-error vector locus after convergence of estimated inductance.

$\boldsymbol{i}_{dest}(k+1)$ is a spatial point that the current vector is scheduled to reach in one sampling period and is a foot of perpendicular from $\boldsymbol{i}^*(k+1)$ on the straight line between $\boldsymbol{i}_{v2}(k+1)$ and $\boldsymbol{i}_{ve}(k+1)$ as illustrated in Fig. 5. The following expressions give the coordinates of $\boldsymbol{i}_{dest}(k+1)$:

$$\boldsymbol{i}_{dest}(k+1) = i_{dest\,\alpha}(k+1) + \mathrm{j} i_{dest\,\beta}(k+1), \tag{9}$$

where

$$\begin{cases} i_{dest\,\alpha}(k+1) \\ = \{v_\alpha^2(k) i_\alpha^*(k+1) + v_\alpha(k) v_\beta(k)[i_\beta^*(k+1) - i_{ve\,\beta}(k+1)] * \\ \qquad * + v_\beta^2(k) i_{ve\,\alpha}(k+1)\} / [v_\alpha^2(k) + v_\beta^2(k)] \\ i_{dest\,\beta}(k+1) \\ = \{v_\beta^2(k) i_\beta^*(k+1) + v_\alpha(k) v_\beta(k)[i_\alpha^*(k+1) - i_{ve\,\alpha}(k+1)] * \\ \qquad * + v_\alpha^2(k) i_{ve\,\beta}(k+1)\} / [v_\alpha^2(k) + v_\beta^2(k)]. \end{cases}$$

The current vector reaching $\boldsymbol{i}_{dest}(k+1)$ makes a current error vector norm minimum at every sampling point.

5) Adjustment of switching sequence and duration

To make the current vector reach $\boldsymbol{i}_{dest}(k+1)$ from $\boldsymbol{i}(k)$, the durations T_{1-6} and $T_{0,7}$ are calculated as follows:

$$\begin{cases} T_{1-6} = \dfrac{\sqrt{[i_{dest\,\alpha}(k+1) - i_{ve\,\alpha}(k+1)]^2 + [i_{dest\,\beta}(k+1) - i_{ve\,\beta}(k+1)]^2}}{\sqrt{2/3} V_{dc}} \hat{L} \\ \qquad = \dfrac{v_{e\,\alpha}(k)[i_{dest\,\beta}(k+1) - i_\beta(k)] - v_{e\,\beta}(k)[i_{dest\,\alpha}(k+1) - i_\alpha(k)]}{v_\alpha(k) v_{e\,\beta}(k) + v_\beta(k) v_{e\,\alpha}(k)} \hat{L} \\ T_{0,7} = T_s - T_{1-6} \end{cases} \tag{10}$$

The inverter output is switched twice in one sampling period and a zero-voltage vector is inserted once a period as shown in Fig. 6. Adopting this switching sequence, the current vector proceeds from $\boldsymbol{i}(k)$ to $\boldsymbol{i}_{dest}(k+1)$ along the scheduled trajectory shown in Fig. 7. The calculation of the durations is affected by variations of the inverter dc-bus voltage and the inductance value set in the controller. The former can be compensated by detecting the real voltage, while the latter must be estimated with an identification mechanism described below.

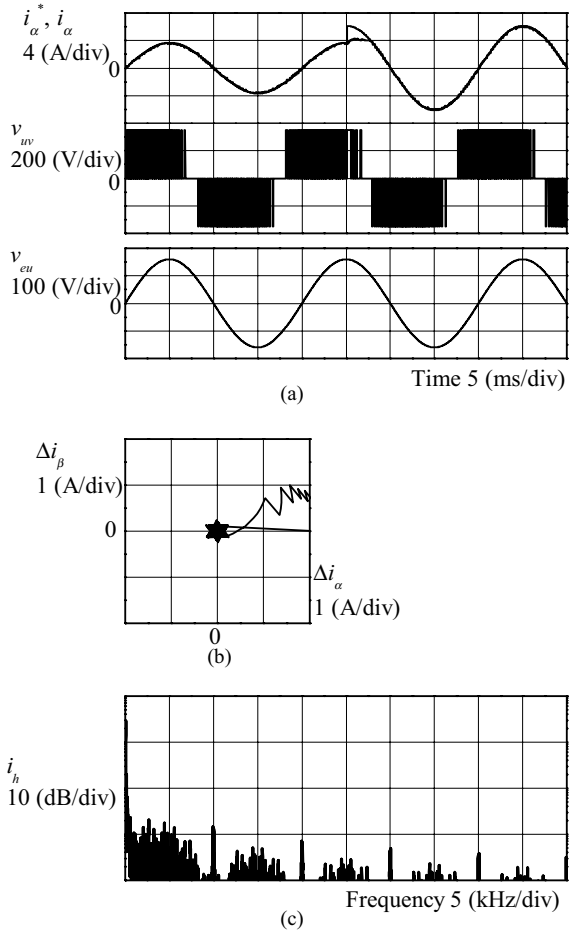

Fig. 10. Simulation result of proposed current controller.
(a) Waveforms of currents, inverter line-to-line voltage and load back e.m.f. (b) Current-error vector locus. (c) Frequency spectra of current.

C. On-Line Identification of Load Inductance

As shown in Fig. 8, identification of the load inductance is performed by evaluating an error between a scheduled destination $\boldsymbol{i}_{dest}(k)$ and an actually reached point $\boldsymbol{i}(k)$. Since the error depends on an inductance mismatch between the controller and the load, the inductance can adaptively be estimated by the following equation, which is based on an integral algorithm with a gain K_I:

$$\hat{L} = K_I \sum [\boldsymbol{i}_{dest}(k) - \boldsymbol{i}(k)]. \tag{11}$$

The above equation represents that the estimated inductance converges to a true value when the error between $\boldsymbol{i}_{dest}(k)$ and $\boldsymbol{i}(k)$ becomes zero.

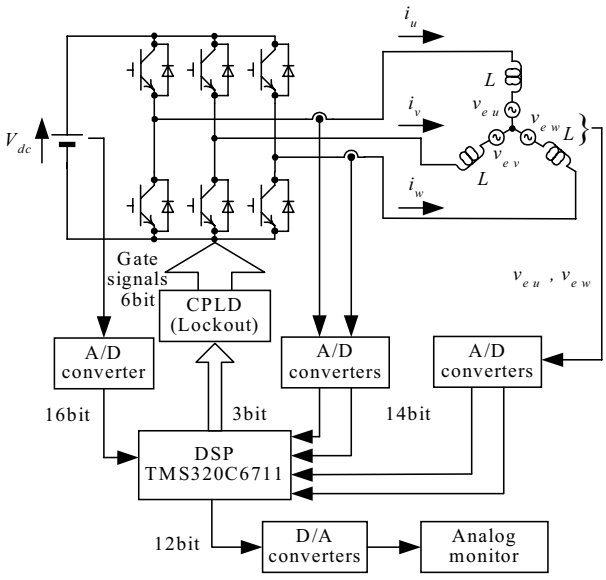

Fig. 11. Schematic diagram of proposed current controller.

III. Computer Simulations and Their Results

A. Test Conditions of Computer Simulation

Several computer simulations have been conducted to examine basic controllability of the proposed method under the condition of $R = 1.0\,(\Omega)$, $L = 50\,(\text{mH})$, $T_s = 100\,(\mu\text{s})$, and $v_e = 160\,(\text{V peak, line to neutral})$. Execution delay time of the proposed algorithm is assumed to be $10\,(\mu\text{s})$ taking actual implementation into account. The inverter's dc-bus voltage is kept constant at $V_{dc} = 350\,(\text{V})$. A lockout circuit function to prevent a short circuit across the dc-bus is introduced in the simulations and its lockout-time is $2.0\,(\mu\text{s})$. The three-phase current commands are obtained from the detected load back e.m.f. and are given to the controller to make the currents in phase with the back e.m.f.

B. Simulation Results of Inductance Identification

Fig. 9(a) shows a characteristic of the inductance identification. The identification was started from an initial value of $10\,(\text{mH})$ and the estimated value asymptotically converged to $53\,(\text{mH})$ approximately after $70\,(\text{ms})$. It is found that the current controllability is remarkably improved as the estimated value converges to the true one in the identification process. This improvement can be verified by the current error vector loci shown in Figs. 9(b) and 9(c).

C. Simulation Results of Current Control

Fig. 10 shows several waveforms of the proposed current controller, where a step response of the current amplitude is included. As can be seen in Fig. 10(a), the phase current follows its current command with a minute error regardless of a sudden change in the current amplitude, which can also be proven by the current error locus shown in Fig. 10(b). The locus indicates a small hexagonal-star-shaped distribution of the current error around the origin although the proposed

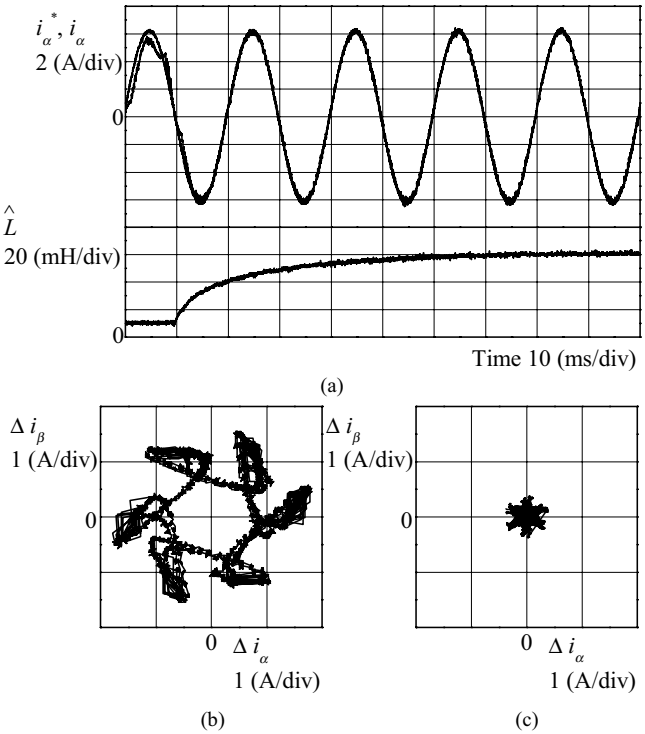

Fig. 12. Experimental result of inductance identification and current-error vector loci.
(a) Waveforms of currents and estimated inductance. (b) Current-error vector locus at initial condition. (c) Current-error vector locus after convergence of estimated inductance.

controller does not have a predetermined current error tolerance. A switching frequency of the inverter is $4\,(\text{kHz})$, which is specified by the sampling period, i.e., $T_s = 100\,(\mu\text{s})$. As shown in Fig. 10(c), however, the current waveform has conspicuous harmonics at $10\,(\text{kHz})$ and its multiples. This profile of the frequency spectra is an advantage to reduce the current harmonics when low-speed switching devices such as GTOs are employed in the inverter.

IV. Experimental Set-up and Its Results

A. Experimental System Set-up

Fig. 11 shows a system configuration of an experimental set-up. The controller consists of full digital hardware employing a digital signal processor (DSP; TMS320C6711) and high-sampling-rate A/D converters (four LTC1414s and one LTC1604). Feedback quantities in this set-up are the phase currents, the load back e.m.f. and the dc-bus voltage of the inverter. The sampling period is set at $100\,(\mu\text{s})$ using one of internal timers in the DSP. Also, another timer is utilized to control timings of the inverter output-voltage vectors, which makes it possible to generate accurate PWM patterns. As described previously, it takes $10\,(\mu\text{s})$ for the DSP to complete the whole calculation needed for the proposed current control. Resultant switching state of the inverter is directly generated by the DSP as 3-bit logic signals and is delivered to an IGBT-based power circuit via a digital lockout circuit integrated with a complex programmable logic device (CPLD), of which lockout-time is $2.0\,(\mu\text{s})$.

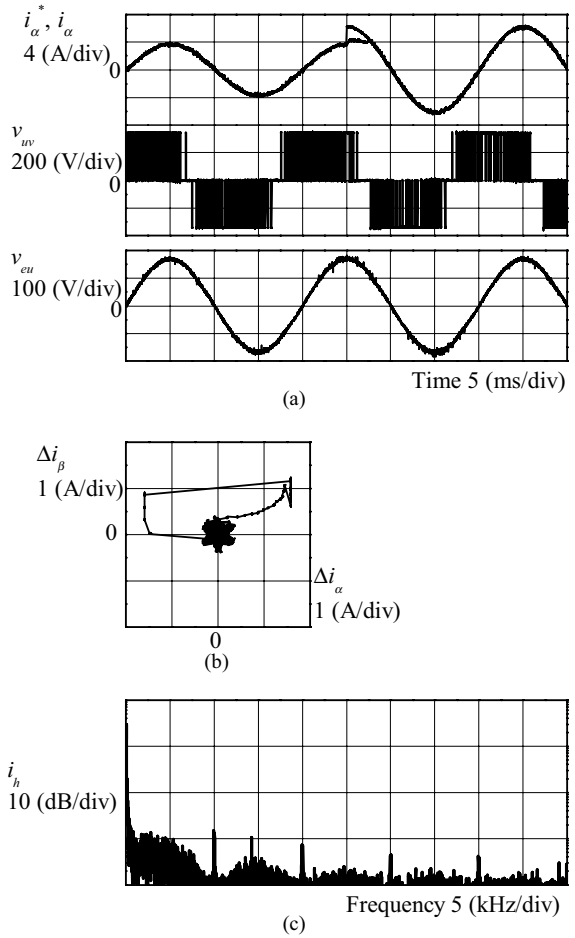

Fig. 13. Experimental result of proposed current controller.
(a) Waveforms of currents, inverter line-to-line voltage and load back e.m.f.
(b) Current-error vector locus. (c) Frequency spectra of current.

B. Experimental Results of Inductance Identification

Fig. 12 shows an experimental result of the inductance identification. Reactors used in the experiment have similar parameter values with those used in the simulation tests. It is observed that the identification is completed approximately in $70\,(\mathrm{ms})$ and that the converged value of the inductance is $61\,(\mathrm{mH})$. Also, the current error is diminished around the origin forming a hexagonal star shape as the estimated inductance converges to the true value as shown in Fig. 12(c). It can be found that the current controllability is also improved as the estimated inductance gradually approaches to the true value.

C. Experimental Results of Current Control

Experimental tests have been conducted under same conditions as those of the simulations. Fig. 13 shows the experimental results.

As can be seen in Fig. 13(a), excellent controllability of the phase current is observed and this fact can be confirmed by the current error vector locus shown in Fig. 13(b). From this figure, it is found that the maximum current error is approximately $0.3\,(\mathrm{A})$ and the current error concentrates around the origin, which means that the steady-state phase and amplitude errors are minute. Fig. 13(c) shows frequency spectra of the phase current measured in the experiment and a conspicuous peak can be found at $10\,(\mathrm{kHz})$, of which result coincides with the frequency spectra profile obtained in the simulation. Also, there can be seen no irregular pulses in PWM patterns of the inverter, which is excellent as well as those of sub-harmonic modulation techniques or space vector modulation techniques. However, the proposed method features dispersed frequency spectra of the phase current regardless of the constant switching frequency of $4\,(\mathrm{kHz})$.

V. Conclusion

This paper described a novel digital current control strategy, which makes it possible to minimize a current error vector norm at every sampling point. The most unique point of the proposed method is to restrict automatically the current error vector within a minute spatial area with no predetermined error tolerance, e.g., a hysteresis band for each phase current or a two-dimensional tolerant area such as a circle. The method achieves optimum PWM patterns, a quick current response, and a small steady-state current error at the same time. Also, it has been clarified that the most conspicuous spectrum of the current harmonics can be observed at a frequency of 2.5-times of the inverter switching frequency. Not only a basic operation of the proposed technique has been examined with computer simulations, but also excellent performances have been confirmed with a prototype through experimental tests.

VI. References

[1] J. Holtz, "Pulsewidth Modulation for Electric Power Conversion," *IEEE Proc.*, **82**, 8, 1194-1214, 1994.

[2] M. P. Kazmierkowski, and L. Malesani, "Current Control Techniques for Three-Phase Voltage-Source PWM Converters: A Survey," *IEEE Trans. on Ind. Elec.*, **45**, 5, 691-703, 1998.

[3] J. Holtz, and S. Stadtfeld, "A Predictive Controller for the Stator Current Vector of AC Machines Fed from a Switched Voltage Source," *Conference Record of 1983 IPEC-Tokyo*, 1665-1675.

[4] T. Kawabata, T. Miyashita, and Y. Yamamoto, "Dead Beat Control of Three-Phase PWM Inverter," *IEEE Trans. on Power Elec.*, **5**, 1, 21-28, 1990.

[5] B. K. Bose, "An Adaptive Hysteresis-Band Current Control Technique of a Voltage-Fed PWM Inverter for Machine Drive System," *IEEE Trans. on Ind. Elec.*, **37**, 5, 402-408, 1990.

[6] K. Ohyama, H. Nakazawa, M. Daijou, T. Yoshida, and Y. Tsunehiro, "A Novel Current Control Technique for Voltage Source Inverter in Field Oriented Control," *IEE-Japan Trans. on Power Elec., Elec. Mach., Power Sys., Energy*, **105-B**, 11, 901-908, 1985.